HIGH SPEED MAGNETIC FIELD GENERATOR

Design Document

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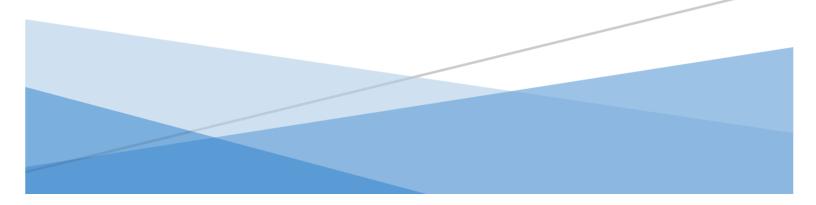


TABLE OF CONTENTS

1	Introduction	4
Pro	plem Statement	4
Pro	ect Purpose	4
Pro	ect Goals	4
2	Deliverables	4
Fall	2016 – EE491	4
Spri	ng 2017 – EE492	5
3	Design	5
Syst	em Specifications	5
r	lon-functional	5
F	unctional	5
Pro	posed Design	5
F	esistors	6
C	apacitors	6
Ľ	Diode	6
L	nductor	6
٨	10SFET	7
Des	ign Analysis	7
C	urrent through the inductor (transmitting coil)	7
S	imulation software limitations	8
4	Testing and Development1	0
Soft	ware and Hardware1	0
S	oftware1	0
ŀ	lardware1	1
5	Measurements1	1

	Coil 1 Test	.12
	Coil 2 Test	.12
6	Future Work	14
	Low-Power Design	.14
	Current-Sense Resistor	.15
7	Conclusions	16
8	References	16
9	Appendix	17
	Importing external SPICE file to NI Multisim	.17

1 INTRODUCTION

PROBLEM STATEMENT

Magnetic field pulse generators have been used for various applications across many different electrical engineering disciplines. Technical requirements of generator systems vary based on the specific application. One of these applications is magneto-optical (MO) switching within fiber optic networks. These networks currently use optical switches and routers to direct signals to desired paths defined by electrical energy. During this process, the conversion from optical energy to electrical energy causes problems. Due to the different bandwidths between optical systems and electrical systems, the signal is not directed to its desired path as quick as needed. However, by utilizing the magneto-optic effect (Faraday effect), the router switching can be achieved without optical-electrical conversion and, consequently, without the high switching latency. One way of inducing the MO effect on the switching system is by applying a strong and quick magnetic field pulse. Past circuit designs have shown that it is possible to create pulse generators with relatively high power and speed. However, there is room for improvement in pulse strength, rise time, and power efficiency.

PROJECT PURPOSE

The purpose of our project is to design and implement a circuit that generates a quicker, stronger pulse while also improving power efficiency. This would provide a more practical way to use magnetic pulse generators in optical switching and higher-scale applications such as transcranial magnetic stimulation (TMS).

PROJECT GOALS

The goals of this project are fourfold:

- 1. Gain a deep, applicable, and robust understanding of magnetic pulse generator concepts and circuit theory that will help us in our future careers and education.
- 2. Build a circuit that can generate a 500 Gauss magnetic field pulse with a rise and fall time of at most, 10 nanoseconds.
- 3. Design and build a low-power version of the pulse generator
- 4. Identify a more effective method of directly measuring the current through the circuit coil

2 DELIVERABLES

The deliverables for our project will be divided between first semester (EE491) and second semester (EE492). Completing these according to our semester timeline will keep us on track to achieve our goals by the end of the year (Spring 2017).

FALL 2016 - EE491

Our final review presentation will cover learning circuit theory and fundamentals, developing PCB fabrication skills, and new circuit modifications/improvements. We will also have two functional circuit boards with us at the final review:

- 1. A board identical to Dec1622 group circuit
- 2. A board with testing points for different current sense resistors

SPRING 2017 – EE492

In April, we will give a presentation on our progress throughout the Spring semester. This will primarily consist of how we built upon the foundation that was established in EE491. We plan on outlining the implementation of our circuit modifications and presenting our solutions to specific problems such as power consumption and measurement techniques. We hope to demo our low-power solution and show how our circuit modifications make test and measurement more accurate and consistent.

3 DESIGN

SYSTEM SPECIFICATIONS

NON-FUNCTIONAL

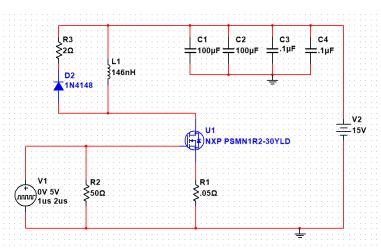
- 1. The product must be on a PCB with a footprint of less than 3.5" x 2"
- 2. The product output must consistent
- 3. The product must be fitted in an insulating enclosure
- 4. The product must have quality soldering for long time using

FUNCTIONAL

- 1. The product shall output a magnetic field pulse peaking at 500 Gauss with rise time of less than 0.15 μ s
- 2. The DC power supply must not exceed 15 V
- 3. The transmitting coil must be fitted for the fiber optic cable

PROPOSED DESIGN





RESISTORS

- The 2 ohm resistor (*Figure 1 R3*) placed series with the diode is used to dissipate some of the energy in its loop. Because there is such a large amount of current flowing through the inductor, this resistor is needed to stabilize the circuit.
- 2. The resistor in parallel with the pulse source (*Figure* 1 R2) is used to match the output impedance of the source. For this source, we are using a Tektronix AFG 3021B function generator which has a 50 ohm output impedance. Matching this impedance is vital in order to prevent signal reflection. In other words, this causes all of the power output of the source to reach the gate of the MOSFET (ideal case).
- 3. The resistor connected to the MOSFET source (*Figure* 1 R1) is used to control the current through the inductor. Because the inductor path can be characterized as an LR circuit, its current pulse characteristics can be controlled through R1. This resistor is also used to measure the current through the inductor (in series with the inductor when the MOSFET is "on" (see *Future Work* section).

CAPACITORS

In order to produce such a high current through the inductor, the circuit needs a dedicated capacitor bank. Our circuit contains a bank of four capacitors in parallel, creating 200.2 μ F of energy storage. The two larger capacitors (C1 and C2) are primarily used to store the charge from the DC source that is eventually sent through inductor, creating the magnetic field. The two smaller capacitors (C3 and C4) act as protection against harmful current spikes. Because the DC source is only 15 V, this capacitor bank is essential in creating the necessary current flow through the coil.

DIODE

The diode placed in series with the resistor can seem as a voltage regulator. We use this diode to make our output stable. The diode can keep a constant voltage at the inductor, so the current through the inductor can be stable, so that the magnetic field pulse from the inductor will be better.

INDUCTOR

The inductor is one of the most important components in our circuit. When calculating the coil's specifications, we have referenced the bottom two equations. Our project requirements are to generate a magnetic field (B) pulse peaking at no less than 500 Gauss with a rise time of no more than $0.15 \ \mu s$. Combining these two requirements essentially defines our current and inductance levels for us, therefore leaving us with specific coil dimensions. For further analysis on this concept, please refer to the *Future Work* section of this document.

$$B = \frac{\mu N I}{\sqrt{l^2 + 4R^2}} \qquad L = \frac{\mu N^2 \pi R^2}{\sqrt{l^2 + 4R^2}}$$

B = magnetic field (Teslas) 1Tesla = 10000 Gauss

L = inductance (Henries)

 μ = permeability of free space ($4\pi \times 10^{-7} H/m$)

N = number of turns in coil

I = current through the coil (Amperes)
l = length of the coil (meters)
R = radius of the coil (meters

MOSFET

Throughout this semester we have used the same MOSFET that the Dec1622 group used over the past year. This led to an easier learning curve because we could get personal help from them. There are certain characteristics of the current MOSFET that are undesirable in some of our future goals. Because of this, we are going to be exploring other MOSFET options in the future, specifically with the low-power solution (see *Future Work* section).

DESIGN ANALYSIS

After researching the concepts behind our circuit, we began simulating the Dec1622 group final circuit. To do this, we had to import the PSMN1R2-30YLD MOSFET made by NXP Semiconductors. This turned out to be quite a challenge because we are using NI Multisim 14.0 as our circuit simulation engine. Multisim does not provide a way to direct import components using a SPICE file (see Appendix). Once we placed the FET, building the circuit was easy and we were able to move onto "playing to learn". In order to gain a deeper understanding of the circuit's functionality, it was vital that we messed with components, changed simulation profiles, and used a variety of sources. This led us to really understand aspects of our circuit like: why we need a diode, how does the MOSFET work and contribute to our goal, and how our inductance and capacitance values dictate the magnetic field output magnitude. Throughout this experimental time, we recorded many scope images that show the behavior of the circuit configuration. In this section, we will outline a few of our most significant findings.

CURRENT THROUGH THE INDUCTOR (TRANSMITTING COIL)

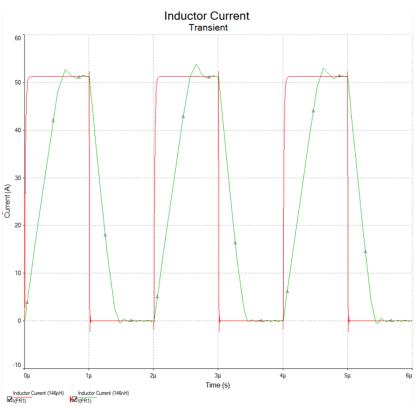


Figure 2

In this graph (Figure 2), you can clearly see the difference between the current drawn through the two different inductors (146nH and 146pH). Although both achieve the desired current level of 50 A, the 146pH inductor has a significantly smaller rise time which is vital for our application. The higher latency of the higher inductance would cause slower switching in an optical fiber network, which is what we are trying to solve. The reasons for these results are somewhat intuitive. Because of the higher inductance, the 146nH indicator takes a lot longer to charge and discharge the current. This change can easily be calculated by using the LR circuit time constant equation:

$$\tau = \frac{L}{R}$$

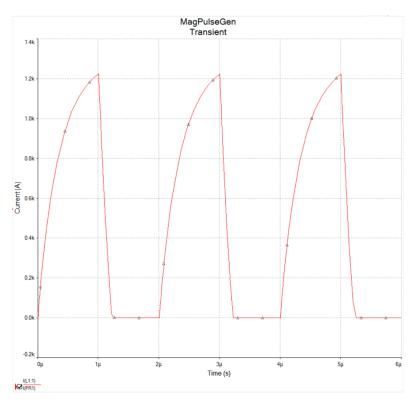
This equation shows the direct relationship between inductance and transient time. It is also known that it takes about 5T to reach steady-state behavior. The challenge of our project is going to be finding a way to achieve a fast rise time while maintaining a sufficient current through the inductor to generate the strong magnetic field. Ideally, when only looking at rise time, smaller inductance is better. However, this decreases the ability to output strong a magnetic field. Furthermore, the physical limitations of our application (fiber optic switching) require a minimum coil diameter which makes *pH*-scale inductances virtually impossible.

SIMULATION SOFTWARE LIMITATIONS

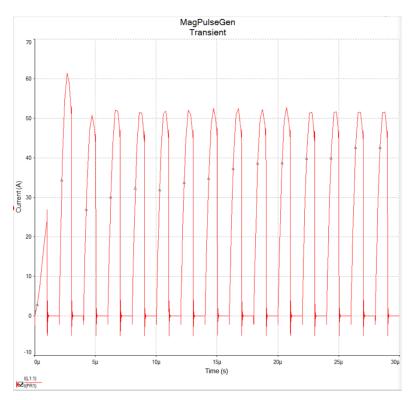
As we experimented with different circuit configurations we found that Multisim has various limitations that make observations difficult to rely on in certain instances.

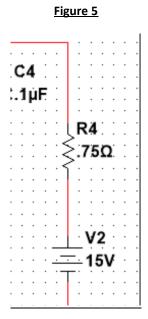
Our first experience with these limitations came when testing the effect of removing the shunt resistor at the source of the FET. Removing this resistor yielded a pretty ridiculous graph (Figure 3) that shows the inductor current peaking at over 1200 A. We know this is impossible for our circuit in real application so we think Multisim is showing its limitation in dealing with truly ideal situations (ideal short between FET source and ground). In order to solve this problem, we attempted to limit the current from the DC course by placing a 0.75 ohm resistor in series (Figure 5). This did, in fact, limit the current of the circuit without the FET source resistor (Figure 4). However, the results show a highly unstable behavior with slow rise and fall times.











Lastly, we have observed a limitation in showing the effects of the charging and discharging of our capacitor bank. We know that our capacitors are meant to store and release charge from the DC source. However, removing the entire capacitor bank from our circuit yields the same exact plot for the current through the inductor as with the capacitors in place. This shows Multisim's inability to show the real-time active behaviors of certain elements.

As we move forward with simulations, our goals are going to be adjusted in order to explore different avenues than the Dec1622 group. One of our main ideas is developing a *low-power* version of the magnetic field generator. We have a few preliminary ideas on how to start on that new path. The big idea is to try to modify the coil in such a way that allows us to draw less current and potentially use lower-powered sources.

4 TESTING AND DEVELOPMENT

SOFTWARE AND HARDWARE

SOFTWARE

Past teams working on this project have used a variety of different software platforms to test and simulate circuit configurations. For our project, we decided to use National Instruments Multisim 14.0 for circuit simulation and National Instruments Ultiboard 14.0 for PCB layout. Our team, in general, has more experience using Multisim from past coursework as opposed to OrCAD PSPICE (used by the Dec1622). Another reason why using PSPICE would not work is that most of our teammates PCs run Windows 10 which causes PSPICE to crash. Our advising team recommended using a Windows 7 PC if we chose to use PSPICE, but eventually decided to go with Multisim.

Once we reached the decision to use Multisim as our simulation platform, we immediately ran into some setbacks. First, we found that there is no direct way to import SPICE file components into a Multisim model. To recreate the Dec1622 group's circuit, we needed to be able to import a MOSFET from NXP Semiconductors which we found on their website in a .lib file format. However, we soon found that it is not possible to load the library file and drop the new component directly into our model. Through extensive online research, we eventually found a roundabout way to use external SPICE components in Multisim (see *Appendix*).

After we decided on the circuit simulation software, it was easy to choose a layout design software. National Instruments has a layout software that works seamlessly with Multisim circuit design called Ultiboard. Furthermore, some of our team members have experience using Ultiboard from EE 333 coursework.

Lastly, we will use MATLAB to build a low-power design model. Ideally, we will be able to graphically show that there is an optimized level of current for a certain time constant. This will show that there is a way to use lower current, and therefore lower power, while maintaining an acceptable rise time.

HARDWARE

We will use all of the standard EE lab equipment to test and evaluate our circuit. Our equipment includes the following:

- Tektronix AFG 3021B Single-channel function generator
- Agilent E3631A DC Power Supply
- Tektronix DPO 4032 Digital Phosphor Oscilloscope
- Various 50 ohm impedance coaxial cables
- Handheld Multimeter
- ISU ECpE Fabrication Drill

5 MEASUREMENTS

Once we had our circuit fabricated, we spent some time testing and measuring its actual behavior. Using simulation software is just a foundation for design, but cannot be relied on when it comes to real-world behavior. Through testing and measurement, we were able to get a clear look at the non-ideal behavior of our circuit. Figure 6 shows our experimental setup for these tests.

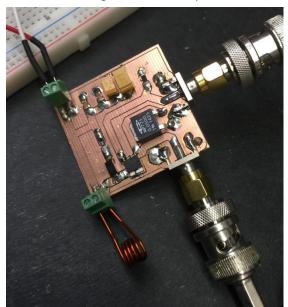
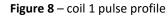


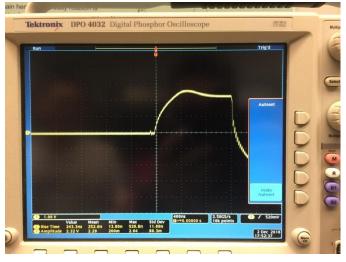
Figure 6 – test setup

COIL 1 TEST

For our first test, we designed a coil with 5 turns and and inductance of about 139 nH (figure 7). This test yielded the pulse seen in figure 8. As a team, we were excited to see a clean plot that shows relatively predictable behavior, however we were not thrilled with the slow rise time.

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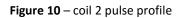


COIL 2 TEST

After seeing decent results for our first coil, we wanted to design a second, smaller, coil (figure 9). We knew that a lower inductance would yield a shorter, more desirable, rise time (figure 10).

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Figure 9 – coil 2 parameters



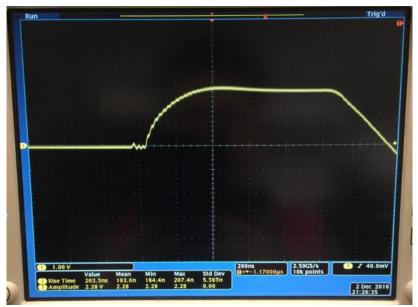
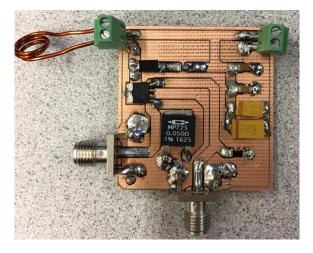
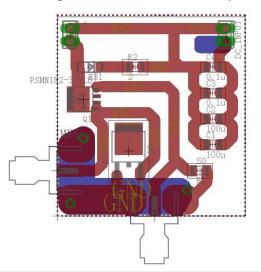


Figure 11 – Main Circuit Board

Figure 12 – Main Circuit Board Layout





 $\frac{BNA}{IR}$

6 FUTURE WORK

Now that we have the foundational concepts of our project, we are confident that we can make significant contributions to the improvement of the magnetic field generator for future MO switching applications. As our project has developed, we have constructed ideas for future improvements to be worked on next semester.

LOW-POWER DESIGN

Fiber optic networks are characterized by rapid data rates with low latency at high efficiency. In order to improve the overall performance of the system, it is necessary for our circuit (MO switch) to be operating at maximum power efficiency. In our application, there are various ways to change the power drawn by the circuit. First, and perhaps the most obvious, is to modify the power sources used in our model. Decreasing the source voltage clearly decreases overall power consumption. Secondly, we can modify other circuit components (resistors, capacitors, MOSFET) in order to draw less current through the coil. This is the method that we are going to pursue next semester because it gives us the most freedom for modifications.

We have started initial calculations to determine the feasibility of this solution. Through this analysis, we believe that we will be able to adjust circuit parameters in order to draw less current through the coil while maintaining pulse magnitude and rise time. Please view our calculations below.

Base Equations:	$\tau = \frac{L}{R}$	$B = \frac{\mu NA}{\sqrt{l^2 + 4R^2}}$	$L = \frac{\mu N^2 A}{\sqrt{l^2 + 4R^2}}$
Calculations:	$L = \frac{\mu N^2 A}{\sqrt{l^2 + 4R^2}} \rightarrow$	$\rightarrow \frac{\mu N}{\sqrt{l^2 + 4R^2}} = \frac{L}{NA} \rightarrow B =$	$\frac{LI}{NA} \rightarrow L = \frac{BNA}{I} \rightarrow \tau =$

Conclusion: 1. const $\tau = \frac{500(NA)\downarrow}{I\downarrow R}$ 2. const $\tau = \frac{500NA}{I\downarrow R\uparrow}$ 3. const $\tau = \frac{500NA\downarrow}{I\downarrow R\uparrow}$

Example: say we want to have a 100 nanosecond rise time. This would make $\tau = 20$ ns since rise time $\approx 5\tau$. To achieve this goal while lower the current through the inductor, we can decrease the dimensions of the coil (method 1). Another way of accomplishing this is to increase the resistance of the circuit through increasing the MOSFET channel resistance and/or the source resistance (method 2). Furthermore, we can combine these two methods to more aggressively counteract the lesser current (method 3).

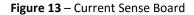
There is no doubt that we still have a lot of work to do in this area next semester, but we believe this solution shows promise and opens the door to other key circuit modifications with the MOSFET and source resistor.

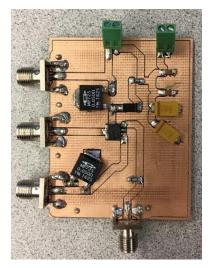
MOSFET: We are finding that the current MOSFET may present challenges to the low-power solution. Tests of our circuit have shown that the FET is operating in its triode region for about 33% of the time and saturation region 66% of the time. Ideally, we could push the FET to saturation in order to tune the channel resistance to a suitable (higher) value for our application. However, we are seeing that in both saturation and triode regions the channel resistance is on the scale of milli-ohms. Because of this, it seems impossible to tune the FET for our low-power scenario. Next semester, we will move forward by searching for a suitable MOSFET for this solution.

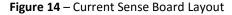
Source Resistor: Our calculations show that we can achieve lower-power solution by increasing the overall resistance of the circuit. As we showed in the previous section, this can be achieved by modifying the MOSFET channel resistance. However, it can more directly be accomplished by increasing the value of the resistor connecting the FET source to ground. Right now, our circuit is generating about 80 W of power in the source resistor that is only rated for 25 W. This poses a problem that we think is causing false data in our measurements. Next semester, we will find a larger resistance rated for a higher power.

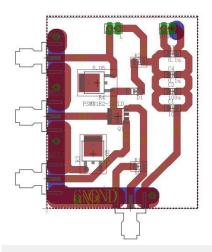
CURRENT-SENSE RESISTOR

The current circuit uses the MOSFET source resistor as a current-sense resistor. However, we believe that placing a small resistor in series directly next to the inductor would provide a more accurate way of measuring inductor current and, therefore, magnetic field strength. We are working on a test board layout that leaves two openings for resistors: one next to the inductor and one connecting the FET source to ground. This will give us an easy way to test our hypothesis that the new resistor placement will lead to better test results. Please find the circuit board and layout of this design below.









7 CONCLUSIONS

In conclusion, we have now caught up to last year's group on our circuit's concepts, functionality, challenges, and purpose. We thoroughly understand the fundamentals of how the circuit works and why we use the components that we do. Now, we are prepared to move forward into the stage of identifying improvements and implementing them. We are confident that by the end of Spring 2017 we will have a new and improved functioning PCB of this magnetic field generator that has been worked on for years.

8 **REFERENCES**

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http://viewer.zmags.com/publication/17fdeoad#/17fdeoad/6

9 APPENDIX

IMPORTING EXTERNAL SPICE FILE TO NI MULTISIM

- 1. Search your package number of MOSFET on google.
- 2. Download the SPICE model on the website
- 3. You will get a page of data about this MOSFET, copy all of them into a new text on your desktop.
- 4. Open NI Multisim
- 5. Select Place->Component
- 6. Copy and paste the package number to the highlighted place

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8. Click the **OK** button to place it on the work area

9. Double left click on the component on the work area and select the Edit Component in dB button

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11. Under Database Name select User Database and then press the Add button

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< opyri <u>c</u>	jht:			_	t model maker

12. Type your package number in the **Model ID** field and click **OK**

Set Parameters	×
Model ID PSMN 1R	2-30YLD
C	OK Cancel

13. Copy the data you saved in the text and paste it to the window under Model data

atabase name:				
Master Database Corporate Database		Add	Delete	
Jser Database		Save	Link info	
		Copy to	Rename	Filter
odel ID list:				
N Manufacturer	Model ID			
1 Generic	PSMN1R2-30YLD			
odel data:				
			**** ^ load	model from file
				model from file
odel data: • NXP PSMN1R2-3 • Polarity N-Ch	0YLD annel			
 NXP PSMN1R2-3 Polarity N-Ch Ratings 30V/1 	OYLD annel .240000E-003OHMS/100A			
NXP PSMN1R2-3 Polarity N-Ch Ratings 30V/1	0YLD annel		Start	
• NXP PSMN1R2-3 • Polarity N-Ch • Ratings 30V/1 • Date Created <	OYLD annel .240000E-003OHMS/100A			
NXP PSMN1R2-3 Polarity N-Ch Ratings 30V/1 Date Created	OYLD annel .240000E-003OHMS/100A		Start	
NXP PSMN1R2-3 Polarity N-Ch Ratings 30V/1 Date Created	OYLD annel .240000E-003OHMS/100A		Start	
NXP PSMN1R2-3 Polarity N-Ch Ratings 30V/1 Date Created	OYLD annel .240000E-003OHMS/100A		Start	

14. Click on the Select button and click the Yes button to change the model data

				Add from comp.
Model name:	PSMN1R2_30YLC			Add/ <u>E</u> dit
	P SPININZ SUTED			Delete a model
				Copy to
	<		>	
Symbol to mo				1
Symbol to mo Symbol pin r	del pin mapping:	Model node name		1
[del pin mapping:	Model node name DRAIN		
Symbol pin r D G	del pin mapping:	DRAIN GATE		
Symbol pin r D	del pin mapping:	DRAIN		

15. Under Model Name select the original model and click the Delete a Model button

eneral symbol Model	Pin parameters Package Electronic parameters User fields	
Component:		
Source location:	User Database / Transistors / Def	
Name:	PSMN1R2-30YLD	
Date:	May 15, 2014	
Author:	NI	
Function:	Single N-Channel MOSFET; 30V; 100A in LFPAK56; Power-SO8	~
	<	>
] This component is o <u>b</u> so	lete	

16. Click on the General tab, type your package number in the Name field

17. In the select Destination Family Name window, select User Database and choose Transistors, and then click Add family, next click OK

Group: Transistors Sources Basic Mise Diodes Consection Analog Mixed Mixed Consection Consect	mily tree:		Database:	User Database
Basic Basic Diodes Analog TTL MCU Add family Mixed Family Family Def Family Month Add family	📴 🎒 User Database	^	Group:	Transistors
Basic Basic Basic Basic Family Family Def Def Def Def Add family Add family Mixed	🕈 Sources		Family:	Def
Diodes If ransistors Analog Analog TTL CMOS MCU Add family Mixed	Masic			
Analog Analog TTL CMOS CMOS ANSI Y32.2 O IEC 60617 Add family Add family Mixed				1 anny
TIL T	📺 🔣 Transistors			
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MCU Advanced_Peripherals Add family Add family				
Image: MCU Image: Misc Digital Image: Misc Digital Image: Misc Digital	CMOS			● ANSI ¥32.2 ○ IEC 60617
🙀 Misc Digital Add family	T MCU			0.000.000
Mixed	Advanced_Peripherals			
	Misc Digital			Add family
	🔐 Mixed			
Indicators Replace component in design	🖪 Indicators		Replace cor	nponent in design
Power V		~		

18. Now when user Place->component, in the user database, the component will be showed and user can place it to the work area

Database:	Co	mponent:	Symbol (ANSI Y32.2)	OK
User Database		SMN1R2-30YLD		OK Close
Group:	P	SMN 1R 2-30YLD	Ť	
All <all groups=""></all>	~			earch
amily:				tail report
All <all families=""></all>	10		<u>⊻</u> i	ew model
Def			*	Help
			Function: Single N-Channel MOSFET; 30V; 100A in LFPAK56; Power-SO8	~
			Model manufacturer/ID:	
			Generic / PSMN 1R2-30YLD	
			Package manufacturer/type:	
			NXP Semiconductors / LFPAK-5(SOT669)	
			Hyperlink:	